Indian J. Phys. **43**, 344–357 (1969)

Coherent generation and reception of frequency shift keyed signals

By A. K. Datta

Physics Department, University of Burdwan, W. Bengal.

(*Received* 3 *April* 1969)

In this paper a few coherent systems for generation and reception of frequency shift keyed signals have been described. It is pointed out that coherent generation will ensure minimum production of transients during change over. A scheme is suggested for correcting Doppler frequency shift automatically. In the method presented, a DSB receiver is adopted for the selection of the upper and the lower sidebands of the transmitted signal. From the experimental results it becomes evident that in regard to the error rate discriminator preceded by a limiter has a decisive advantage over the one without the limiter.

Introduction

In frequency shift keying (FSK) the frequency of the transmitted signal is keyed or altered in accordance with a digital sequence obtained from the analogue message. In binary FSK, for example, this involves the transmission of energy at two slightly different frequencies for the mark and the space signalling conditions. The generally accepted convention is to transmit for the mark state a frequency slightly higher than that for the space state. Each mark and the space state has got a fixed duration. One, therefore, can write for the frequencies of these two states $f_1 = f_0 + f_d$ c/s and $f_2 = f_0 - f_d$ c/s where f_1 and f_2 correspond to the frequencies of the mark and the space signalling conditions respectively, spaced $2f_d$ cycles apart; f_d is called the deviation or shift in frequency from the centre frequency f_0 which is the arithmetic mean of the two shifted frequencies f_1 and f_2.

A possible mathematical representation for a binary FSK signal is

$$e_k(t) = A\cos[\omega_o \pm \omega_d]\, t \qquad \text{...... Type I}$$

$$\text{or } e_k(t) = A/2[\cos(\omega_1 t + \phi_1) - \cos(\omega_2 t + \phi_2)]$$

$$+ x.\, A/2[\cos(\omega_1 t + \phi_1) + \cos(\omega_2 t + \phi_2)]$$

where the subscript k is either 1 or 2 and x is a random quantity which can have values either $+1$ or -1.

This shows that a binary FSK wave can be viewed as the sum of two steady state cosine waves given by the first term and a random component given by the second term in the above expression. The random component can be identified as a binary FSK (phase shift keying) wave at two different carrier frequencies f_1 and f_2. So far as the intelligence is concerned the power associated with the steady cosine waves is a waste and can be compared with the carrier power in AM. Discriminator, detection (analogus to envelope detection in AM.) is possible because of the presence of this steady component. Suppression of this power in the transmitter requires the implementation of coherent detection technique in the receiver and in such circumstances the signal can be represented simply as

$$e_k(t) = x.\ A/2[\cos(\omega_1 t + \phi_1) + \cos(\omega_2 t + \omega_2)] \qquad \text{...... Type II}$$

FSK signal may be of two distinguishing types, (i) discontinuous phase (switching between two oscillators) and (ii) continuous phase (switching the frequency of a single oscillator). In the former, two very stable sources at frequencies f_1 and f_2 are incorporated in the transmitter and during transmission either of these sources may be selected and switched on as desired. In the latter, two state frequencies are derived from a single source. The usual technique is to use digital sequence directly for frequency modulating a voltage controlled oscillator (VCO). Whatever be the technique implemented in generating, it has to be ensured that switching ON and OFF, either from one source to the other or the same to the other or the same source between two frequencies should be instantaneous and the periods for build up and decay of oscillations should be as small as possible. Otherwise, there will be overlapping intervals within a bit period causing unwanted interference leading to misinterpretation on faulty decision of the transmitted state in the receiver.

The techniques of generation described in this paper give due consideration to the above facts and ensure a good degree of reliability in the system. The bit period is chosen so as to accommodate an integral number of rf cycles irrespective of the state of the transmitted message. Switching is done at the instants when the rf voltage passes through zero level. The keying signal is derived from the reference source itself thereby the switching instants are determined a-priori. The techniques employed in the present study may be classified as (i) sideband selection (ii) controlled scaling, (iii) feed forward, (iv) feedback and (v) phase lock type. In section 2 the proposed methods of generation of FSK signals have been dealt with in a greater detail.

With regard to reception of FSK signal emphasis in the present paper will be on semi-coherent techniques of detection rather than on incoherent (or discriminator) detection. In section 3, a scheme is described for correcting Doppler frequency shift in which a SBPL type receiver is adopted. In section 4, various aspects of receiving FSK signal have been dis cussed assuming the noise free received signal. In receiving FSK signal of the type I mentioned earlier one can either make use of single CPL circuit centred at the assigned carrier frequency f_0 or two CPL circuits at the state frequencies with 'hold' in the control circuit. For FSK signal of the type II one can use a SBPL circuit centred at the state frequencies for the same. The effects of the presence of additive noise and other transmission impairment have been studied in section 5. Experimental set-up and findings have been presented in section 6.

Coherent generation of FSK signal

Frequency shift keying of oscillator usually produces switching transients causing undesirable sideband components. Proper selection of the switching instant commensurate with the bit period, bit rate and the frequencies of the two state voltages will greatly reduce these effects thereby cross talks on other subcarrier channels will be minimised. Elimination of these transients reduces frequency transition time, permitting a high keying rate. The work of Sunde (1959) has indicated that the special case in which $2f_d = 1/T$ where T is the bit period has a theoretical advantage in that the intersymbol interference can be suppressed at the sampling instants in the output of an ideal frequency detector. According to Bennet & Rice (1963) if there is a commensurate relationship between the making, the spacing and the signalling frequencies such as to produce continuous phase at the transitions, the spectral density varies as the inverse fourth power of frequency and if in addition the derivative of the phase is also continuous, the spectral density varies as the inverse sixth power of frequencies beyond the two state frequencies.

In this section we shall describe different techniques of generating FSK signals in a coherent manner. The methods described can be classified as (i) Controlled Scaling, (ii) Sideband Selection, (iii) Feedback, (iv) Feed Forward and (v) Phase Lock type of generation.

Sideband Selection :

In the method referred to as sideband selection the system mainly consists of a carrier oscillator (a highly stable rf source), a frequency divider, a pair of balanced modulator and an adder stage. The keying signal and accordingly the shift in frequency is derived from the carrier sources (f_0) by frequency division. A reference to figure 1 will show that the output of the modulator I, may be represented by $mA\cos \omega_0 t . \cos \omega_d t$. The output of the modulator II may be represented by $mA\sin \omega_0 t . \sin\omega_d t$. This can be had by feeding the modulator II, with a quadrature carrier and a quadrature modulating signal and the polarity reversal (i.e., $\pm$ sign) can be obtained by feeding the modulating signal either directly or a phase inverted version of it to the modulator. The term quadrature is referred here in respect of the corresponding components in the modulator I. The modulating signal feeding the modulator II is keyed between 'directly' or 'inverted' in accordance with the message to be transmitted.

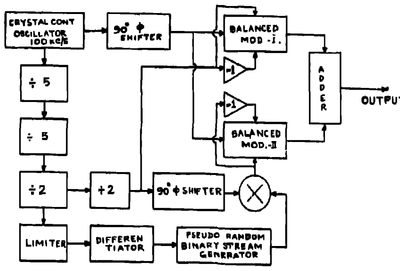

Figure 1. Block diagram of a coherent scheme of FSK generation using 'Sideband Selection' technique.

Controlled Scaling

In the method referred to as controlled scaling use is made of a highly stable rf source (X-tal controlled) to derive the mark space frequencies and the switching over signal. Thereby the time duration for the mark or space signals are clocked with the reference oscillation and change over can occur at the scheduled instants of time. The heart of this system is the controlled scaling unit. The internal logic of the scaling unit is altered to have two different counts for the mark and space states, respectively. The operation of the system is explained with a reference oscillator at 9,999 Kc/s, from which trigger pulses at the same rate are derived. The trigger pulses are fed to a selection or scaling circuit; the scaling factor by which the input pulse train are scaled down is either 99 or 101. Thus the selection circuit gives out 101,000 or 99,000 trigger pulses in a second which are ultimately converted into rectangular (or pulsed) voltage waveform The voltages thus obtained can be given a sinusoidal shape by passing through appropriate filter networks. The selection between 99 or 101 is done in accordance with the state of the message to be transmitted. The switching over signal is also derived from the reference oscillation keeping in mind that change over is allowed at those instants of time as discussed earlier for which the generation of transients are limited to a minimum.

Feed Forward and Feed Back Techniques

In controlled scaling method of FSK signal generation the internal logic (i.e., scaling factor) of the scaling unit is changed, whereas, in these techniques the scaling factor is kept unchanged but additional pulses generated from the input pulse train are added to the input and thus the number of pulses coming out of the scaling unit in a given time is changed. In feed forward technique the incoming pulse train is fed in parallel to a divider and the scaling unit. The other input to the scaler is the output pulses from the divider which are accepted by means of a control circuit. In feedback type, from the output of the scaler a number of pulses are generated which are fed in parallel with incoming pulse train to the scaler.

Phase Lock Type

The phase lock method of generation (figure. 2) mainly consists of an automatic phase control (APC) circuit. The VCO incorporated in the APC unit is locked in phase with either of the two reference inputs (f_1 and f_2) depending on the state of the message. The reference inputs are derived either from two very stable sources or from a single source following either of the techniques mentioned earlier. Such a system will ensure very good phase stability of the state outputs well within a bit.

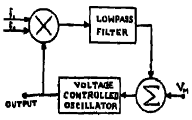

Figure 2. Block diagram of a coherent scheme of ESK generation using 'Phase Locking' technique.

Adoption of A DSB receiver for correcting Doppler frequency shift for signal reception

The technique of sideband phase locking has been dealt with in detail in a previous commnication (Charkrabarti *et al* 1966). In this section we shall describe how a DSB receiver using sideband phase locking technique can be adopted for the reception of narrowband FS-keyed signal.

Establishing Locking of the Reference Carrier in the Receiver

It has been mentioned that a coherent receiver derives the necessary controlling voltage for establishing coherence of its local oscillator (a voltage controlled type), from the received signal itself. The received signal may be represented for FSK modulation as $Ak\cos(\omega_k t + _k)$, where the subscript $k = 1$ for the mark signalling condition and $k = 2$ for the space signalling state ; A_k, ω_k, and ϕ_k are the respective amlitude, angular frequency and the phase of the received signal. A reference to figure. 3 will show that incoming signal is split into two channels each of which contains

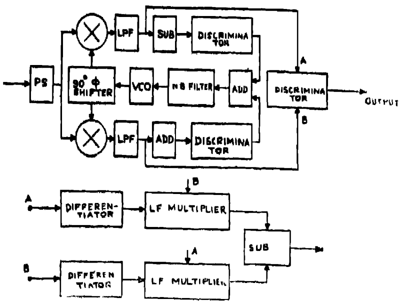

Figure 3. Block diagram of the scheme for correcting Doppler frequency shift in receiving FSK signal using a SBPL type reccIver.

a product demodulator. The demodulating carriers in the demodulators are derived from the same VCO incorporated in the receiver but are in phase quadrature with each other $e_p(t) = B\cos(\omega_0 t + \psi_0)$ and $e_q = B\sin(\omega_0 t + \psi_0)$. The low frequency outputs accepted by means of low pass filters following the demodulators may be written as

$$P_1(t) = K\cos(\omega_d t + \phi_1 - \psi_0)$$

$$\text{and } Q_1(t) = -K\sin(\omega_d t + \phi_1 - \psi_0)$$

in the P and Q channels, respectively, for the mark signalling condition and

$$P_2(t) = K\cos(\omega_d - \phi_2 + \psi_0)$$

$$\text{and } Q_2(t) = K\sin(\omega_d t - \phi_2 + \psi_0)$$

in the P and Q channels, respectively, for the space signalling conditions

The outputs $P(t)$'s and $Q(t)$'s are given phase shifts θ_P and θ_Q such that $\theta_P \sim \theta_Q = \pi/2$. The two phase shifted outputs thus obtained are then added together or subtracted from each other to make use of the discriminators following the respective adder and subtractor stages.

It is therefore clear from the above equations for $P(t)$'s and $Q(t)$'s that the existence of an output on addition shows the presence of space signalling condition at that moment. On the other hand the existence of an output on subtraction indicates the mark state of the received signal. It may further be added in this context that when an output is obtained on addition implies no output on subtraction and *vice versa*.

In the above it is tacitly assumed that the reference carrier in the receiver is in frequency synchronism with the assigned carrier in the transmitted signal. In case when there is a discrepancy between the two (*i.e.*, $f_{lo} \neq f_o$) the frequency of the local oscillator can be supposed as $f_{lo} = f_o \pm \Delta f_o$; entailing a frequency $f_h = f_d \mp \Delta f_o$, in the mark channel output and a frequency $f_l = f_d \pm \Delta f_o$, in the space channel output. It is thus seen that a discrepancy $+ \Delta f_o$ in the frequency of the injected carrier causes a decrease in frequency in the mark channel output by the same amount, whereas, the frequency of the output in the space channel is increased by the same factor. The use of a voltage controlled oscillator in the receiver enables one to circumvent the aforesaid discrepancy in frequency. The necessary controlling voltage can be obtained from a frequency discriminator operated by the outputs of the adder and subtractor stages.

It may be thought that if the outputs of the mark and space channels are applied to a discriminator of centre frequency f_d the output from the discriminator may be used to control the frequency of the local oscillator. This is not possible because of an inherent ambiguity. For one must know which channel is being received at the moment in order to fix the polarity of the controlling voltage. A little thought will show that the following conditions are to be satisfied.

Channel received		Discrepancy in frequency	Conclusion
Mark	Space		
$f_h<f_d$	$f_l>f_d$	positive ($+\Delta f_o$)	Reduce L. O. frequency
$f_h>f_d$	$f_l<f_d$	negative ($-\Delta f_o$)	Increase L. O. frequency

To get rid of the difficulty mentioned earlier it is needed to use two discriminators followed by the adder or the subtractor stages, respectively, in the mark and space channels. The characteristics of the discriminators should have the nature shown in figure 4. The outputs of these two discri-

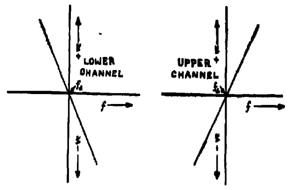

Figure 4. Shows the required characteristics for the discriminators.

minators are added and used to control the frequency of the local oscillator so as to decrease the phase discrepancy ϕ and if possible to eliminate it.

Recognition of the Mark and Space Signalling States

When locking of the demodulating carrier is established by the estimation channel in the receiving system, the low frequency outputs of the P and Q channels can be written as

$$P_1(t) = K \cos(\omega_d t + \theta)$$

and $$Q_1(t) = -K \sin(\omega_d t + \theta)$$

respectively for the mark signalling state of the received signal and that for the space state can be written as

$$P_2(t) = K \cos(\omega_d t + \theta)$$

and $$Q_2(t) = K \sin(\omega_d t + \theta).$$

The outputs of the P and Q channels are fed to a low frequency discriminator which gives at its output a dc voltage in proportion to the frequency of its inputs. The polarity of this voltage depends on the state of the incoming signal and gives the keying information. The demodulator is identified as the demodulation discriminator.

Design and Fabrication

In the following sections we shall discuss the design and fabrication of some of the important components of the reception system discussed. The most important components of such a reception system are the low frequency discriminators *viz.* (i) estimation discriminator and (ii) demodulation discriminator. The relevant points in fabricating the discriminators are discussed below.

Estimation Discriminator

Phase frequency characteristic of a null network may profitably be utilised in building low frequency discriminiators having the desired characteristics. A reference to figure 5 will show that it consists of a LCR bridge and a product circuit. The voltage that will be developed across RC combination can be shown to be proportional to sin ϕ where ϕ is the phase difference between the output voltage of the null network and its input. The parameters are to be so chosen as to have a null or zero output at a frequency equal to the shift in frequency f_d. It is known that the magnitude of the phase ϕ depends on the difference of the frequency of the input signal with that of its null frequency and the sign of the phase depends on whether the input frequency is higher or lower than the null frequency of the network. To have the desired characteristic of the second one an additional phase shift of 180° is to be introduced to the signal before it is fed to the null network.

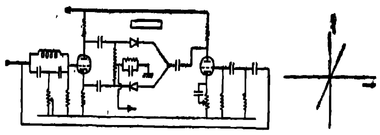

Figure 5. Circuit diagram of the discriminator unit used in the estimation channel together with its frequency-voltage characteristic.

Demodulation Discriminator

A reference to figure 6 will show that the demodulation discriminator essentially consists of differentiators, multipliers and a subtractor. The component parts are to be so designed as to give reliable performance at a frequency as low as 100 c/s. It can be shown that the discriminator output is given by $\pm D\omega_d$. where D takes account of all the constants *viz.* constant of the differentiator and that of the multiplier.

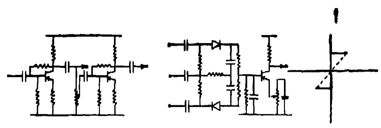

Figure 6. Circuit diagram of the discriminator unit used in the demodulation together with its frequency-voltage characteristic.

Reception of F-S keyed signals

In this section we shall discuss various techniques of receiving FSK signals and in particular coherent scheme of detection. We consider first the case of noise free reception. The effects of noise will be dealt with in a subsequent section. The identification of the incoming state of the received signal may be carried out using (i) incoherent (or discriminator) detection and (ii) coherent detection.

In the former, the receiving system consists of two identical channels, each channel containing a bandpass filter centred at one of the state frequencies followed by an envelope detector. The outputs of the envelope detectors are subtracted from each other and the difference output is sampled. The decision of the received state is made from the polarity of this sampled output. Performance of such a receiving system becomes very unpredictable and unreliable in presence of channel perturabtions caused by various transmission impairments (e. g., the Doppler shift). In such circumstances a coherent system will have a decisive advantage and may be behaving quite faithfully, of course, within certain bounds.

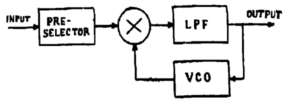

Figure 7. Block diagram of CPL type receiving unit for the reception of FSK signal.

A coherent system essentially consists of a feedback controlling loop which operates on the received signal (irrespective of the state) and derives the necessary controlling voltage for the purpose of gaining coherence and maintaining synchronism. In receiving FSK signal of the type I mentioned earlier one can make use of a single CPL circuit centred at the arithmetic mean of the two shifted frequencies for controlling the phase of the VCO automatically. But in such circumstances it is to be ensured that the loop bandwidth is so adequate that the oscillator is able to follow up the change in frequency in each bit interval and attains a steady state within a reasonable time compared to the bit interval. The input to the system is given by $A\cos(\omega_o + x\,\omega_d)$ t. A reference to the figure 7 will show that the output of the low pass filter is given by

$$e_d(t) = K\,G(s)\sin(x\omega_d t - \phi)$$

This output is used to control the frequency of the VCO and to keep the discrepancy to a minimum.

$$\frac{d\phi}{dt} = K\,G(s)\sin(x\,\omega_d t - \phi)$$

For small phase error

$$S\phi = K\,G(s)\,(x\,\omega_d t - \phi)$$

$$\text{or, } \phi = \frac{K\,G(s)\,x\,\omega_d t}{S + K\,G(s)}\,.$$

$$\text{or, } (x\,\omega_d t - \phi) = \frac{x\,\omega_d}{S + K\,G(s)}\,.$$

The expression for $e_d(t)$ now changes to

$$e_d(t) = \frac{xKG(s).\,\omega_d}{S + K\,G(s)}\,.$$

While receiving FSK signal of the type II using an SBPL circuit we refer the input to the system as

$$e_i(t) = xA\,(\cos\omega_1 t + \cos\omega_2 t).$$

A reference to the figure 3 will show that the outputs of the P and Q

channels are given by

$$e_P(t) = x\, K\, G(s) [\cos(\omega_d t - \phi) + \cos(\omega_d t + \phi)]$$

and $$e_Q(t) = x\, K\, G(s) [\sin(\omega_d t + \phi) - \sin(\omega_d - \phi)].$$

The controlling voltage in this case is given by $e_d(t) = < e_P(t).e_Q(t) > = K_1 \sin 2\phi$. Under locked condition $\phi = 0$ which gives $e_P(t) = 0$ and $e_Q(t) = K, G(s).\, x.\, \sin \omega_d t$. This output is sampled at the bit interval where overlap is minimum. The sampled output is then tested for the polarity. Keyed integration and destructive sampling may give a still better result.

In coherent detection, the bandpass filters are followed by product demodulators with demodulating carriers in phase with either the assigned carrier or the state frequencies. The low frequency outputs of the demodulators are accepted by means of low pass filters following the demodulators. Now the decision of the received state may be made in either of the two ways (i) the outputs of the low pass filters are integrated and sampled and the decision is made from a comparison of the magnitude of the sampled output and (ii) the outputs of the low pass filters are subtracted from each other and integrated output is sampled and the decision is made from the polarity of the sampled output. Sampling should be done at the proper instants of time to achieve a maximum gain in SNR and from this consideration it is preferred to choose the sampling instant at the middle of the bit interval. At the two extremities of a bit interval there is much ambiguity in deciding exact state because of the interfering effect of the preceding and the following bits.

Effects of noise and other interferences

In this section we shall consider the effects of the noise in the reception band in causing error in decision. We shall assume the noise to be additive in nature and white, gaussian in character with zero mean.

In the CPL case the input to the system in the presence of noise is given by

$$e_i(t) = A \cos(\omega_0 \pm \omega_d)t + n_c \cos \omega_0 t + n_q \cos \omega_0 t.$$

where n_c and n_q are the in phase and quadrature components of the noise. Both n_c and n_q are white, gaussian independent variables.

The output of the VCO is given by $B \sin(\omega_0 t + \phi_n)$ where the phase discrepancy ϕ_n is a slowly varying quantity. The output of the low pass filter is given by

$$\begin{aligned} e_d(t) &= K [A \sin(\phi_n \mp \omega_d t) + n_c \sin \phi_n + n_q \cos \phi_n] \\ &= K [(\mp A \sin \omega_d t + n_q) \cos \phi_n + n_c \sin \phi_n]. \end{aligned}$$

An error occurs when the sample value of $A \sin \omega_d t + n_q$ gives a polarity indication opposite to that of $A \sin \omega_d t$.

In the SBPL case the input to the system is given by
$e_i(t) = \pm A\,[\cos(\omega_o + \omega_d)t + \cos(\omega_o - \omega_d)t] + n_c \cos\omega_o t + n_q \sin\omega_o t.$
The demodulating carriers in this case are given by

$$B\cos(\omega_o t + \phi_n) \text{ and } B\sin(\omega_o t + \phi_n).$$

The P and Q channel outputs are given by

$$x\,AB\,[\cos(\omega_d{}' - \phi_n) + \cos(\omega_d t + \phi_n)] + n_c B \cos Q_n - n_q B \sin Q_n'$$

and $x\,AB\,[-\sin(\omega_d t - \phi_n) + \sin(\omega_d t + \phi_n)] + n_c B \sin\phi_n + n_q B \cos\phi_n]$.
The controlling voltage is given by

$$e_d(t) = K \sin 2\phi + n_c n_q\, B\cos 2\phi$$

which shows that the effect of noise in the controlling voltage is felt as a cross modulation term. The very appearence of the noise in this form will boost up low frequency spectral density, as a consequence of which the states will be held up. The bandwidth occupancy of the output noise will also increase. This high frequency boosting up of the spectral density will cause a larger number of change of states. A reference to the product output shown in figure 8 where a PR sequence of length fifteen will support the statement mentioned above.

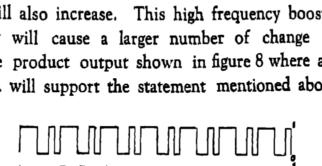

Figure 8. At the bottom is depicted the product output between two pseudo random sequences of length seven (at the top) and of length fifteen (in the middle).

Experimental set-up and discussions

A laboratory model of the system (transmitter and receiver) was constructed and tested. Here we shall mainly discuss the principal features of the different component units and a few experimental findings.

A. *Transmitter*

It mainly consists of a modulator (FM oscillator) and a modulating source generating a random binary pattern. A psuedo-random (PR) sequence generator of length fifteen was constructed using switching transistors (type 2N404). Performance of the sequence generator was satisfactory for switching rate upto 54 Kc/s.

An rf oscillator at 2.0 Mc/s was frequency modulated using the output of the sequence generator as the keying signal. The deviation was adjusted to a proper value comensurate with the repetition rate.

B. *Receiver*

Discriminator detection was made to get a comparative study with that of an APC type detection. In the discriminator detection it was tried i) with limiting and ii) without limiting cases in regard

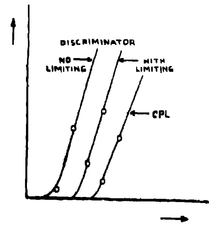

Figure 9. Shows the variation of number of errors recorded in (i) discriminator detection with and without limiting and (ii) in APC type reception.

to output SNR and error rates in presence of additive noise at the receiver. APC filter was constructed at a frequency equal to the assigned carrier *i.e.*, at 2.0 Mc/s. Effect of filtering the output of the demodulator in regard to the output SNR and error rate was also studied.

In measuring the error rates, the transmitted sequence was first reconstructed (following filtering, amplifying and hard limiting in a Schmidt circuit) from the demodulated output and then the Mod-2 sum of the recostructed sequence and the transmitted sequence was sampled at the middle of the bit and coincidence is detected. A counter following the AND circuit directly counts the number of erroneously received bit in a given period (present time). In respect of discriminator detection measurements of errors were made for the (i) limiting and (ii) without limiting cases with the level of the input noise and is plotted in figure 9. The figure also depicts the variation of the number of erroneously received bit with the level of the input noise for APC type detection.

Concluding Remarks

A detailed study of the experimental findings elucidating the principal objectives of the work will be presented in a future communication.

In discriminator detection it is observed that limiting, in general, improves the performance as regards the error rate and the threshold SNR. The automatic phase control type of reception using carrier and sideband phase locking techniques is particularly suitable when the received signal undergoes Doppler frequency shift. When it is not possible to achieve phase locking in the prevailing circumstances it is hoped that differentially coherent detection, where a currently received pulse may be stored and used to demodulate the pulse arriving in the next time slot, may be utilised with profit.

In recording errors there are objections to the use of non-liner processing in the Schmidt trigger. A few alternative schemes may be as follows.

(a) The received sequence is sampled (bipolar sampling) at T/2. The sampled pulse is multiplied with the complement of the reference sequence and pulses of only one polarity are accepted.

(b) The received sequence is sampled at $T/2$ and the sampled values are held to reconstruct the delayed sequence. The reference sequence is delayed by $T/2$ by means of a shift register. Mod-2 sum of the two sequences thus obtained is tested for the polarity.

(c) Both the received and the reference sequences are sampled. The sampled outputs are multiplied.

(d) Received sequence and the transmitted reference sequence are multiplied and integrated. The integrator output is sampled at time T_1 and tested for polarity.

(e) Mod-2 sum of the delayed received sequence and the complement of transmitted sequence is tested for polarity.

Arrangement (d) can be used for measuring both bit error and word error by adjusting the prf of the sampling pulse.

The author expresses his gratitude to Prof. N. B. Chakrabarti of I. I. T., Kharagpur for supervision of the work reported in this paper and for his valuable guidance in the preparation of the manuscript. The author wishes to thank Prof. G. S. Sanyal, Head, Department of Electronics and Electrical Communication Engineering, I. I. T., Kharagpur for his kind interest and constant encourangement also for the kind permission to work in the Department.

References

Bennet, W. R. & Rice, S. O. 1963 *B. S. T. J.* **42**, 2355.

Chakrabarti, N. B. & Datta, A. K. 1966 *Indian J. Phys.* **40**, 501.

Sunde, E. D. 1959 *B. S. T. J.* **38**, 1337.